****

**EE 4550L**

**IC Hardware Security and Trust LAB**

**SPRING 2024**

**TA: Kanchan Vissamsetty**

**Lab section: 01**

**Name: Alex Yeoh**

**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Alex Yeoh Date: 15th March 2024**

**Report due date: 15th March 2024**

1. **OBJECTIVE**

To learn how to perform Monte Carlo analysis with Cadence.

1. **PROCEDURE**

Build the desired circuits using the components that can be used to simulate with Monte Carlo analysis and perform the simulation with the relevant Monte Carlo analysis model libraries.

1. **RESULT**

**A graph with lines and text

Description automatically generated with medium confidence**

Waveform for the 4-bit full adder without trojan with the best and worst delays labeled.

A graph of a graph

Description automatically generated with medium confidence

Waveform for the 4-bit full adder with trojan with the best and worst delays labeled.

|  |  |  |
| --- | --- | --- |
| Worst Delays Table | | |
| Output | Without Trojan | With Trojan |
| S1 | None with the given inputs | None with the given inputs |
| S2 | 194.6154ps | 196.2781ps |
| S3 | 64.73653ps | 64.73829ps |
| S4 | None with the given inputs | None with the given inputs |

Table of worst delays for each input

Question 1: Because Monte Carlo analysis simulates PVT variations.

Question 2: The S3 output for the trojan-attacked design has a very slight increase in delay. Outputs S1 and S4 maintain constant for both designs so they have no delay, but the trojan-attacked S4 has a more pronounced glitch.

1. **CONCLUSION**

My results satisfy the requirements. I don’t think I can improve my design to get better results. I have learned how to perform Monte Carlo analysis in Cadence.